

PATENT

Attorney Docket No.: 8733.721.00-US

UNITED STATES PATENT APPLICATION

OF

HAE JIN YUN

FOR

**THIN FILM TRANSISTOR ARRAY SUBSTRATE AND MANUFACTURING
METHOD THEREOF**

**MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, N.W.
WASHINGTON, D.C. 20006
TEL: (202) 496-7500
FAX: (202) 496-7756**

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to thin film transistor array substrates. More particularly, this invention relates to thin film transistor array substrates, and to their manufacturing methods, having reduced data pad and data link contact resistances.

Description of the Related Art

[0002] A liquid crystal display (LCD) uses electric fields to control the light transmittance through a liquid crystal to produce an image. To this end, an LCD includes a liquid crystal display panel having a matrix of liquid crystal cells, and driving circuits for driving the liquid crystal cells.

[0003] In a liquid crystal display panel, gate lines and data lines are arranged in a crossing manner. Liquid crystal cells are formed in areas defined by the crossing gate and data lines. The liquid crystal display panel includes pixel electrodes and a common electrode for producing electric fields from the liquid crystal cells. Each pixel electrode is selectively connected, via source and drain electrodes of a thin film transistor that acts as a switching device, to a data line. The gate electrode of each thin film transistor is connected to a gate line. Scanning signals applied on the gate lines switch pixel voltage signals on the data lines to the pixel electrodes.

[0004] The driving circuits include a gate driver for driving the gate lines, a data driver for driving the data lines, and a common voltage generator for driving the common electrode. The gate driver sequentially applies scanning signals to the gate lines to sequentially drive the liquid crystal cells line-by-line. The data driver applies data voltage signals (also referred to as pixel voltage signals) to the data lines when a scanning signal is applied to a gate line. The common voltage generator applies a common voltage to the common electrode. Accordingly, the LCD changes alignment states of the liquid crystal between the pixel electrodes and the common electrode in response to the pixel voltage signals on the pixels to control light transmittance, thereby displaying a picture.

[0005] For instance, an LCD having a thin film transistor array substrate is shown in Fig. 1. Fig. 2 shows a sectional view of the thin film transistor array substrate of Fig. 1 taken along line A-A'. As shown in those figures, the thin film transistor array substrate includes a gate line 2 and a data line 4 on a lower substrate 34. The gate and data lines 2 and 4 cross each other. A gate insulating film 36 is disposed between the gate and data lines 2 and 4. A thin film transistor 6 is provided at the intersection of the gate and data lines 2 and 4. A pixel electrode 16 is provided at a liquid crystal cell area defined by the gate and data lines 2 and 4.

[0006] The thin film transistor 6 includes a gate electrode 8 that is connected to the gate line 2, a source electrode 10 that is connected to the data line 4, a drain electrode 12 that is connected to the pixel electrode 16, and an active layer 14 that overlaps the gate electrode 8. The active layer selectively defines a channel between the source electrode 10 and the drain electrode 12. The active layer 14 is overlapped by the data line 4, by the source electrode 10, and by the drain electrode 12. An ohmic contact layer 38 for making an ohmic contact with the data line 4, with the source electrode 10, and with the drain electrode 12 is provided on the active layer 14. The thin film transistor 6 allows a pixel voltage signal applied to the data line 4 to be applied to the pixel electrode 16 in response to a gate signal applied to the gate electrode 8.

[0007] The pixel electrode 16 is electrically connected via a first contact hole 18 through a protective film 40 to the drain electrode 12. A voltage applied to the pixel electrode 16 and the potential applied to the common electrode on an upper substrate (not shown) produce an electric field. That electric field rotates a liquid crystal between the thin film transistor array substrate and the upper substrate owing to dielectric anisotropy. This controls the light from a light source (not shown) that passes to the upper substrate.

[0008] The gate line 2 is connected, via a gate pad portion 20, to a gate driver (not shown,), while the data line 4 is connected, via the data pad portion 28, to the data driver (not shown). The gate pad portion 20 is comprised of a gate pad 24 that is extended from the gate line 2, and a gate pad protection electrode 25 that is connected, via a plurality of second contact holes 26 through the gate insulating film 36 and through the protective film 40, to the gate pad 24. The data pad portion 28 is comprised of a data pad 30 that is extended by way of a data link 5 from the data line 4, and of a data pad protection electrode 31 that is connected, via a plurality of third contact holes 32 through the protective film 40, to the data pad 30.

[0009] Hereinafter, a method of fabricating the thin film transistor substrate having the above-mentioned structure using a five-round mask process will be described in detail with reference to Fig. 3A to Fig. 3E. Referring to Fig. 3A, gate patterns are provided on the lower substrate 34. To do so, a gate metal layer is formed on the lower substrate 34 by a deposition technique such as sputtering. Then, the gate metal layer is patterned by photolithography using a first mask and an etching to produce the gate patterns. A gate pattern includes the gate line 2, the gate electrode 8, and the gate pad 24. The gate metal is beneficially a single-layer or double-layer structure of chrome (Cr), molybdenum (Mo), or an aluminum group metal.

[00010] Referring to Fig. 3B, the gate insulating film 36, the active layer 14, and the ohmic contact layer 38 are then provided on the lower substrate 34 with the gate patterns. To do so, the gate insulating film 36, an amorphous silicon layer, and an n⁺ amorphous silicon layer are sequentially provided by deposition techniques such as plasma enhanced chemical vapor deposition (PECVD) or sputtering. Then, the n⁺ amorphous silicon layer and the amorphous silicon layer are simultaneously patterned by photolithography using a second mask and an etching process. The gate insulating film 36 is beneficially comprised of an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x).

[00011] Referring to Fig. 3C, source/drain patterns are then formed on the structure illustrated in Fig. 3B. To do so, a source/drain metal layer is formed using a deposition technique such as sputtering. Then, the source/drain metal layer is patterned by photolithography using a third mask and an etching process to form the source/drain patterns. Each source/drain pattern includes a data line 4, a source electrode 10, a drain electrode 12, and a data pad 30. Then, the ohmic contact layer 38 between the source electrode 10 and the drain electrode 12 is removed by a dry etching. This separates the source electrode 10 and the drain electrode 12. The source/drain metal is beneficially made from molybdenum (Mo), titanium (Ti), tantalum (Ta), a molybdenum alloy, or chrome (Cr).

[00012] Referring to Fig. 3D, a protective film 40 having contact holes 18, 26 and 32 is then formed on the structure shown in Fig. 3C. To do so, a protective film material is formed by a deposition technique such as plasma enhanced chemical vapor deposition (PECVD). The protective film material is then patterned by photolithography using a fourth mask and a dry etching process to define the first to third contact holes 18, 26 and 32. As shown, the first contact hole passes through the protective film 40 and through the data

electrode to expose the ohmic contact layer 38. The second contact holes 26 pass through the protective film 40 and the gate insulating film 36 to expose the gate pad 24. The third contact holes 32 pass through the protective film 40 and through the data pad 30 to expose the ohmic contact layer. The protective film 40 is beneficially comprised of an inorganic material that is identical to that used to form the gate insulating film 36, or of an organic material having a small dielectric constant, such as an acrylic organic compound, BCB (benzocyclobutene), or PFCB (perfluorocyclobutane).

[00013] Referring to Fig. 3E, transparent electrode patterns are then provided on the protective film 40. To do so, a transparent electrode material is deposited onto the protective film 40 by a deposition technique such as sputtering. Then, the transparent electrode material is patterned by photolithography using a fifth mask and an etching process to provide the transparent electrode patterns, each of which includes a pixel electrode 16, a gate pad protection electrode 25, and a data pad protection electrode 31. As shown, the pixel electrode 16 is in side contact with the drain electrode 12 via the first contact hole 18, the gate pad protection electrode 25 is in surface contact with the gate pad 24 via the second contact holes 26, and the data pad protection electrode 31 is in side contact with the data pad 30 via the third contact holes 32. The transparent electrode material is formed from indium-tin-oxide (ITO), tin-oxide (TO), or indium-zinc-oxide (IZO).

[00014] In the described conventional method of manufacturing a thin film transistor array substrate, when molybdenum (Mo), which is easily dry etched, is used as the source/drain metal, the contact holes 18 and 32 are formed through the drain electrode 12 and through the data pad 30. Thus, the pixel electrode 16 and the data pad protection electrode 31 formed over the contact holes 18 and 32 are in side contact with the drain electrode 12 and with the data pad 30. As a result, since the side contact area is narrow, the contact resistance between the drain electrode 12 and the pixel electrode 16, and the contact resistance at the data pad portion 28, produce signal quality deterioration.

[00015] In the described thin film transistor array substrate, each data pad 30 is connected via a data link 5 to a data line 4. However, the data links 5 have different lengths in accord with their positions. This is because the data links 5 connect closely spaced data pads 30 to widely spaced data lines 4. The different data link lengths produce link resistance differences that can cause distortion of the pixel voltage signals.

[00016] The above-mentioned thin film transistor array substrate also can be made using a four-round mask process. This beneficially reduces the number of manufacturing processes that are required. Typically, a four-round mask process uses a diffractive exposure mask to pattern the semiconductor layers (including the amorphous silicon layer and the n⁺ amorphous silicon layer) and the source/drain metal layer using a single mask.

[00017] More specifically, the semiconductor layer and the source/drain metal layer are disposed on a substrate. Then, a photo-resist pattern having different thicknesses in the source/drain pattern portion and in the channel portions is provided by photolithography using a mask having a diffractive exposing part. In particular, the photo-resist pattern formed by the diffractive exposing technique (in the channel portions) is thinner than the source/drain pattern portion. Subsequently, the substrate is patterned by a wet etching process. Then, the thinner photo-resist pattern is removed from the channel portion by an ashing process. Thereafter, the source/drain metal layer and the n⁺ amorphous silicon layer of the channel portion are etched by a dry etching process. A stripping process then removes the remaining photo-resist pattern.

[00018] In such a four-round mask process, when the photo-resist pattern of the channel portion is removed by the ashing process, an accident can occur in which the photo-resist pattern at the data pad portion is removed. Therefore, when the source/drain metal layer and the n⁺ amorphous silicon layer of the channel portion are etched by a dry etching process, the data pad is subject to removal. This can result in an open defect at the data pad portion.

SUMMARY OF THE INVENTION

[00019] Accordingly, it is an object of the present invention to provide a thin film transistor array substrate, and its manufacturing method, wherein the data pad is formed from a metal layer that is different than the source/drain patterns. This can reduce contact resistance.

[00020] A further object of the present invention is to provide a thin film transistor array substrate, and its manufacturing method, wherein the data link is formed from a double metal layer that reduces link resistance.

[00021] A still further object of the present invention is to provide a thin film transistor array substrate, and its manufacturing method, wherein the data pad is formed from a metal layer that is different than that of the source/drain patterns.

[00022] To achieve these and other objects of the invention, a thin film transistor array substrate according to one aspect of the present invention includes a pixel electrode in each liquid crystal cell; thin film transistors that are connected to the pixel electrodes; crossing gate lines and data lines that are connected to the thin film transistors; gate pad portions for electrically connecting to a gate driver; data pad portions for electrically connecting to a data driver; gate link portions connected between the gate pad portions and the gate lines; and data link portions connected between the data pad portions and the data lines. The data pad portions each include a data pad protection electrode and a data pad. The data link portions include a first data link that extends from the data pad, and a second data link that extends over the first data link. The first data link is formed from a metal layer that is different than that used to form the data line to which it will be electrically connected. That connection is via a contact electrode that extends from the second data link to the data line.

[00023] In the thin film transistor array substrate, the data pad and the first data link are formed from the same gate metal layer as the gate line. The data line is formed from the source/drain metal layer.

[00024] The contact electrode, the second data link, and the pixel electrode are formed from the same transparent conductive material.

[00025] The data pad protection electrode is in surface contact with the data pad via contact holes through the gate insulating film and through the protective film over the data pad.

[00026] The contact electrode is connected, via contact holes through the protective film, to the data line, and, via contact holes through the gate insulating film and the protective film, to the first data link.

[00027] A method of manufacturing a thin film transistor array substrate according to another aspect of the present invention includes forming a gate line and a data line that intersect each other with a gate insulating film therebetween, forming a thin film transistor near the intersection of said two lines, forming a gate link and a gate pad that extend from the gate line, forming a data pad provided at a different layer from the data line, and forming a first data link that extends from the data pad. Then, forming a protective film on the entire

structure, and thereafter defining a plurality of contact holes through the protective film. Then, forming a pixel electrode that is connected via a first contact hole to the thin film transistor, a gate pad protection electrode that is connected via second contact holes to the gate pad, a data pad protection electrode that is connected via third contact holes to the data pad, a second data link extends along the first data link from the data pad protection electrode, and a contact electrode that extends from the second data link and that connect to the first data link and to the data line via fourth and fifth contact holes.

[00028] The method includes depositing a gate metal material onto the substrate and then patterning it to form a gate electrode of the thin film transistor, a gate line, a gate pad, a data pad and the first data link. Also, forming the gate insulating film; depositing a semiconductor material on the gate insulating film, and then patterning the semiconductor material to form an active layer and an ohmic contact layer of the thin film transistor. Also, depositing a source/drain metal material and patterning it to form source and drain electrodes of the thin film transistor and the data line.

[00029] Alternatively, the method depositing a gate metal material onto the substrate and then patterning it to form a gate electrode of the thin film transistor, a gate line, a gate pad, a data pad and the first data link. Then, forming the gate insulating film and depositing a semiconductor material and a source/drain metal material. Then, patterning the semiconductor material and the source/drain metal material to form an active layer, an ohmic contact layer, source and drain electrodes of the thin film transistor, and the data line.

[00030] In the method, the data pad protection electrode is formed in surface contact with the data pad via contact holes through the gate insulating film and through the protective film on the data pad. The contact electrode is connected, via contact holes through the data line and through the protective film, to the data line, while also being connected, via contact holes through the gate insulating film and through the protective film to the first data link.

BRIEF DESCRIPTION OF THE DRAWINGS

[00031] These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

[00032] Fig. 1 is a plan view showing a portion of a thin film transistor array substrate of a conventional liquid crystal display;

[00033] Fig. 2 is a sectional view of the thin film transistor array substrate of Fig. 1 taken along line A-A';

[00034] Fig. 3A to Fig. 3E are sectional views that are helpful for illustrating a method of manufacturing the thin film transistor array substrate shown in Fig. 1 and in Fig. 2;

[00035] Fig. 4 is a plan view showing a portion of a thin film transistor array substrate according to an embodiment of the present invention;

[00036] Fig. 5 is a sectional view of the thin film transistor array substrate of Fig. 4 taken along lines B-B' and C-C';

[00037] Fig. 6A to Fig. 6D are views that are helpful for illustrating a method of manufacturing the thin film transistor array substrate shown in Fig. 4;

[00038] Fig. 7A to Fig. 7D are sectional views that are helpful for illustrating a method of manufacturing the thin film transistor array substrate shown in Fig. 4;

[00039] Fig. 8 is a plan view showing a structure of a thin film transistor array substrate according to another embodiment of the present invention;

[00040] Fig. 9 is a sectional view of the thin film transistor array substrate of Fig. 8 taken along lines D-D' and E-E';

[00041] Fig. 10A to Fig. 10E are plan views that are helpful for illustrating a method of manufacturing the thin film transistor array substrate shown in Fig. 8; and

[00042] Fig. 11A to Fig. 11E are sectional views that are helpful for illustrating a method of manufacturing the thin film transistor array substrate shown in Fig. 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[00043] Fig. 4 and Fig. 5 are a plan view and a sectional view showing a structure of a thin film transistor array substrate according to an embodiment of the present invention. That embodiment is beneficially fabricated using a four-round mask process. The thin film transistor array substrate includes a gate line 52 and a crossing data line 54 on a lower substrate 92. A gate insulating film 94 is disposed between the crossing lines. Additionally, a thin film transistor 56 is provided at the intersection of the crossing lines, and a pixel electrode 66 is provided at a liquid crystal cell area defined by the crossing lines.

[00044] The thin film transistor 56 includes a gate electrode 58 that is connected to the gate line 52, a source electrode 60 that is connected to the data line 54, a drain electrode

62 that is connected to the pixel electrode 66, and an active layer 64 that overlaps the gate electrode 58. The active layer is for defining a channel between the source electrode 60 and the drain electrode 62. The active layer 64 is overlapped by the data line 54, by the source electrode 60, and by the drain electrode 62. An ohmic contact layer 96 for making ohmic contacts with the data line 54, with the source electrode 60, and with the drain electrode 62 is on the active layer 64. The thin film transistor 56 allows a pixel voltage signal that is applied to the data line 54 to be selectively applied to the pixel electrode 66 in response to scanning signals applied to the gate line 52.

[00045] The pixel electrode 66 is connected, via a first contact hole 68 through a protective film 98, to the drain electrode 62. The pixel electrode 66 is for producing an electric field to a common electrode on an upper substrate (not shown) when a pixel voltage is on the pixel electrode. That electric field rotates a liquid crystal between the thin film transistor array substrate and the upper substrate owing to a dielectric anisotropy. This enables control of light from a light source that is applied to the upper substrate.

[00046] The gate line 52 is connected, via the gate pad portion 70, to a gate driver (not shown,) while the data line 54 is connected, via the data pad portion 80, to a data driver (not shown). The gate pad portion 70 is comprised of a gate pad 72 that is extended from the gate line 52, and a gate pad protection electrode 78 that is connected, via a plurality of second contact holes 76 through the gate insulating film 94 and through the protective film 98, to the gate pad 72. The data pad portion 80 is comprised of a data pad 82 that is connected, via a contact electrode 89 and via a data link portion, to the data line 54, and of a data pad protection electrode 86 that is connected, via a plurality of third contact holes 90 through the protective film 94, to the data pad 82.

[00047] The data pad 82 and a first data link 84 are formed from a gate metal layer. The first data link 84 is electrically connected via a contact electrode 89 and via fourth and fifth contact holes 57 and 87 to the data line 54. The data line 54 is formed from the source/drain metal layer. The data pad protection electrode 86 is formed from a transparent electrode layer. Also formed from the transparent electrode layer are a second data link 88 that overlaps the first data link 84 and the contact electrode 89. The protective film 98 is between the first data link 84 and the second data link 88. Such a parallel conductive structure (the first data link 84 formed from a gate metal layer and the second data link 88 formed from

a transparent electrode layer) can reduce the link resistance over the single conductive structure of the prior art.

[00048] Furthermore, the data pad 82 it is in surface contact with the data pad protection electrode 86 via the third contact holes 90 that pass through the protective film 98 and through the gate insulating film 94. Thus, the contact area between the data pad 82 and the data pad protection electrode 86 is greater than in the side contacts of the prior art.

[00049] Moreover, as the data pad 82 is formed from a gate metal layer, erosion of the data pad 82 by a dry etching process can be prevented by using the fabrication process that is subsequently described. Hence defects in the data pad portion 80 can be reduced or prevented.

[00050] Hereinafter, a method of fabricating the thin film transistor array substrate shown in Fig. 4 and Fig. 5 using a four-round mask process will be described in detail with reference to Fig. 6A to Fig. 6D, which are plan views of the thin film transistor array substrate, and with reference to Fig. 7A to Fig. 7D, which are sectional views.

[00051] Referring now to Fig. 6A and to Fig. 7A, gate patterns are provided on the lower substrate 92. To do so, a gate metal layer is formed on the upper substrate 92 by a deposition technique such as sputtering. Then, the gate metal layer is patterned by photolithography using a first mask and an etching process. Each set of gate patterns includes a gate line 52, a gate electrode 58, a gate pad 72, a data pad 82, and the first data link 84. The gate metal beneficially is a single-layer or double-layer structure of chrome (Cr), molybdenum (Mo), or an aluminum group metal.

[00052] Referring now to Fig. 6B and to Fig. 7B, the gate insulating film 94, the active layer 64, the ohmic contact layer 96, and the source/drain patterns are sequentially formed on the lower substrate 92 having the gate patterns. To do so, the gate insulating film 94, an amorphous silicon layer, an n⁺ amorphous silicon layer, and the source/drain metal layer material are sequentially disposed. Then, a photo-resist pattern is formed on the source/drain metal layer by photolithography using a second mask. The second mask is a diffractive exposure mask having a diffractive exposing part where the channel portion of the thin film transistor is to be. This enables the photo-resist pattern at the channel portion to be thinner than other places.

[00053] Subsequently, the source/drain metal layer is patterned by a wet etching process using the photo-resist pattern. This forms source/drain patterns, each of which

includes a data line 54, a source electrode 60, and a drain electrode 62 that is integral with the source electrode 60. The data line 54 partially overlaps the first data link 84.

[00054] Next, the n⁺ amorphous silicon layer and the amorphous silicon layer are patterned using a dry etching process and the same photo-resist pattern. This forms the ohmic contact layer 96 and the active layer 64.

[00055] The thin portion of the photo-resist pattern is then removed (from the channel portion) by an ashing process. Thereafter, the source/drain pattern and the ohmic contact layer 96 of the channel portion are etched by a dry etching process. Thus, the active layer 64 of the channel portion is exposed and the source electrode 60 and the drain electrode 62 are separated. The data pad 82 formed from the gate metal layer is protected by the gate insulating film 94. This prevents accidental erosion of the data pad 82 by the dry etching process. A stripping process then removes the remaining photo-resist pattern.

[00056] The gate insulating film 94 is beneficially comprised of an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x). The source/drain metal is beneficially comprised of molybdenum (Mo), titanium (Ti), tantalum (Ta), a molybdenum alloy, or chrome (Cr).

[00057] Referring now to Fig. 6C and to Fig. 7C, the protective film 98 with contact holes 68, 76, 90, 57, and 87 is then formed on the structure with the source/drain patterns. To do so, the protective film material is formed using a deposition technique such as plasma enhanced chemical vapor deposition (PECVD). The protective film material is then patterned by photolithography using a third mask and an etching process to define the first to fifth contact holes 68, 76, 90, 57 and 87. The first contact hole 68 passes through the protective film 98 and through the drain electrode 62. The second contact holes 76 pass through the protective film 98 and through the gate insulating film 94 to expose portions of the gate pad 72. The third contact holes 90 pass through the protective film 98 and through the gate insulating film 94 to expose the portions of the data pad 82. The fourth contact holes 57 pass through the protective film 98 and through the data line 54. The fifth contact holes 87 pass through the protective film 98 and through the gate insulating film 94 to expose portions of first data link 84. The protective film 98 is beneficially comprised of an inorganic material that is the same as the gate insulating film 94, or of an organic material having a small dielectric constant, possibly an acrylic organic compound, BCB (benzocyclobutene), or PFCB (perfluorocyclobutane).

[00058] Referring now to Fig. 6D and Fig. 7D, transparent electrode patterns are then provided on the protective film 98. To do so, a transparent electrode material is deposited onto the protective film 98 by a deposition technique such as sputtering. Then, the transparent electrode material is patterned by photolithography using a fourth mask and an etching process to provide the transparent electrode patterns. Each transparent electrode pattern includes a pixel electrode 66, a gate pad protection electrode 78, a data pad protection electrode 86, a second data link 88, and a contact electrode 89.

[00059] Still referring to 6D and to Fig. 7D, the pixel electrode 66 is electrically connected, via the first contact hole 68, to the drain electrode 62. The gate pad protection electrode 78 is electrically connected, via the second contact holes 76, to the gate pad 72. The data pad protection electrode 86 is electrically connected, via the third contact holes 90, to the data pad 82. The contact electrode 89 is extended by way of the second data link 88 from the data pad protection electrode 86 and electrically connects the data line 54 to the first data link 84 through the fourth and fifth contact holes 57 and 87. The data pad protection electrode 86 is in surface contact with the data pad 82, thereby reducing contact resistance. The transparent electrode material is formed from indium-tin-oxide (ITO), tin-oxide (TO), or indium-zinc-oxide (IZO).

[00060] As described in the method of manufacturing the thin film transistor array substrate according to the present invention, the data pad 82 is formed from a gate metal layer. Thus, it is possible to prevent erosion of the data pad 82 by the dry etching process that removes the source/drain pattern and the ohmic contact layer.

[00061] Fig. 8 and Fig. 9 are a plan view and a sectional view showing a structure of a thin film transistor array substrate according to another embodiment of the present invention. That thin film transistor array substrate is formed using a five-round mask process. Referring to Fig. 8 and to Fig. 9, the thin film transistor array substrate includes a gate line 102 and a data line 104 on a lower substrate 142 in such a manner that they intersect each other with a gate insulating film 94 disposed between them. A thin film transistor 106 is provided at the intersection. A pixel electrode 116 is provided at a liquid crystal cell area defined by the crossing lines.

[00062] The thin film transistor 106 includes a gate electrode 108 that is connected to the gate line 102, a source electrode 110 that is connected to the data line 104, a drain electrode 112 that is connected to the pixel electrode 116, and an active layer 114 that

overlaps the gate electrode 108. The active layer 114 is for providing a channel between the source electrode 110 and the drain electrode 112. The active layer 114 is overlapped by the data line 104, by the source electrode 110, and by the drain electrode 112. An ohmic contact layer 146 for making ohmic contacts with the data line 104, with the source electrode 110, and with the drain electrode 112 is provided on the active layer 114. The thin film transistor 106 allows a pixel voltage signal applied to the data line 104 to be applied to the pixel electrode 116 in response to a gate signal applied to the gate line 102.

[00063] The pixel electrode 116 is connected, via a first contact hole 118 through a protective film 148, to the drain electrode 112 of the thin film transistor 106. The pixel electrode 116 is for producing a potential difference with respect to a common electrode on an upper substrate (not shown) when a pixel voltage is applied to the pixel electrode 116. This potential difference produces an electric field that rotates a liquid crystal between the thin film transistor array substrate and the upper substrate owing to a dielectric anisotropy. This controls the light from a light source (which is not shown) that passes to the upper substrate.

[00064] The gate line 102 is connected, via the gate pad portion 120, to a gate driver (not shown), while the data line 104 is connected, via the data pad portion 130, to a data driver (not shown). The gate pad portion 120 is comprised of a gate pad 122 that is extended by way of a gate link from the gate line 102, and of a gate pad protection electrode 128 that is connected, via a plurality of second contact holes 126 through the gate insulating film 148 and through the protective film 144, to the gate pad 122. The data pad portion 130 is comprised of a data pad 132 that is connected, via a contact electrode 139 and via a data link portion, to the data line 104, and of a data pad protection electrode 136 that is connected, via a plurality of third contact holes 140 through the protective film 144, to the data pad 132.

[00065] The data pad 132 and the first data link 134 are formed from a gate metal layer. The first data link 134 is electrically connected, via the contact electrode 139 and via fourth and fifth contact holes 107 and 137, to the data line 104. The data line 104 is formed from a source/drain metal layer. The data pad protection electrode 136 is formed from a transparent electrode layer. The second data link 138 and the contact electrode 139 are also formed from the transparent electrode layer. The contact electrode overlaps the first data link 134 and is on the protective film 148. Such a parallel connection structure comprised of the first data link 134, which is formed from a gate metal layer, and the second data link 138,

which is formed from a transparent metal layer, can reduce the link resistance in comparison to the single structure used in the prior art.

[00066] Furthermore, the data pad 132, which is formed from the gate metal layer, is in surface contact with the data pad protection electrode 136 via third contact holes 140 through the protective film 148 and through the gate insulating film 144. Thus, the contact area between the data pad 132 and the data pad protection electrode 136 is increased, thereby reducing contact resistance in comparison to the prior art (which used a side contact).

[00067] A method of fabricating the thin film transistor substrate shown in Fig. 8 and Fig. 9 using a five-round mask process will be described with reference to Fig. 10A to Fig. 10E, which are plan views, and to Fig. 11A to Fig. 11E, which are sectional views of the thin film transistor array substrate.

[00068] Referring now to Fig. 10A and Fig. 11A, gate patterns are provided on the lower substrate 142. To do so, a gate metal layer is formed on the upper substrate 142 by a deposition technique such as sputtering. Then, the gate metal layer is patterned by photolithography using a first mask and an etching process to form gate patterns. Each gate pattern includes a gate line 102, a gate electrode 108, a gate pad 122, a data pad 132, and a first data link 134. The gate metal beneficially is a single-layer or double-layer structure of chrome (Cr), molybdenum (Mo) or an aluminum group metal.

[00069] Referring now to Fig. 10B and Fig. 11B, the gate insulating film 144, the active layer 114, and the ohmic contact layer 146 are formed on the lower substrate 142 having the gate patterns. To do so, the gate insulating film 144, an amorphous silicon layer, and an n⁺ amorphous silicon layer are sequentially formed. Subsequently, the n⁺ amorphous silicon layer and the amorphous silicon layer are etched by photolithography using a second mask and an etching process to form the ohmic contact layer and the active layer 114. The gate insulating film 144 is made from an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x).

[00070] Referring now to Fig. 10C and Fig. 11C, source/drain patterns are then formed on the gate insulating film 144 provided with the active layer 114 and with the ohmic contact layer 146. To do so, a source/drain metal layer is formed by a deposition technique such as sputtering. Subsequently, the source/drain metal layer is patterned by photolithography using a third mask and an etching process to form source/drain patterns. Each source/drain pattern includes a data line 104, a source electrode 110, and a drain

electrode 112. The data line 104 partially overlaps the first data link 134. Then, the ohmic contact layer 146 between the source electrode 110 and the drain electrode 112 is removed by a dry etching process. This electrically isolates the source and drain electrodes 110 and 112. The source/drain metal is beneficially comprised of molybdenum (Mo), titanium (Ti), tantalum (Ta), a molybdenum alloy, or chrome (Cr).

[00071] Referring now to Fig. 10D and to Fig. 11D, the protective film 148 having contact holes 118, 126, 140, 107, and 137 is then formed. To do so, a protective film material is provided over the structure having the source/drain metal layers by a deposition technique such as plasma enhanced chemical vapor deposition (PECVD). The protective film material is then patterned by photolithography using a fourth mask and an etching process to define the first to fifth contact holes 118, 126, 140, 107 and 137.

[00072] Still referring to Fig. 10D and to Fig. 11D, the first contact hole 118 passes through the protective film 148 and the drain electrode 112. The second contact holes 126 pass through the protective film 148 and through the gate insulating film 144 to expose portions of the gate pad 122. The third contact holes 140 pass through the protective film 148 and through the gate insulating film 144 to expose portions of the data pad 132. The fourth contact holes 107 pass through the protective film 148 and through the data line 104. The fifth contact holes 137 pass through the protective film 148 and through the gate insulating film 144. The protective film 148 is beneficially comprised of an inorganic material that is identical with the gate insulating film 94, or of an organic material having a small dielectric constant, such as an acrylic organic compound, BCB (benzocyclobutene), or PFCB (perfluorocyclobutane).

[00073] Referring to Fig. 10E and Fig. 11E, transparent electrode patterns are then provided on the protective film 148. To do so, a transparent electrode material is deposited on the structure having the protective film 148 by a deposition technique such as sputtering. Then, the transparent electrode material is patterned by photolithography using a fifth mask and an etching process to provide the transparent electrode patterns. Each transparent electrode pattern includes a pixel electrode 116, a gate pad protection electrode 128, a data pad protection electrode 136, a second data link 138 and a contact electrode 139.

[00074] Still referring to Fig. 10E and to Fig. 11E, the pixel electrode 116 is electrically connected, via the first contact hole 118, to the drain electrode 112. The gate pad protection electrode 128 is electrically connected, via the second contact holes 126, to the

gate pad 128. The data pad protection electrode 136 is electrically connected, via the third contact holes 140, to the data pad 132. The contact electrode 139 is extended by way of the second data link 138 from the data pad protection electrode 136. The contact electrode 139 electrically connects the data line 104 to the first data link 134 via the fourth and fifth contact holes 107 and 137. As shown, the data pad protection electrode 136 is in surface contact with the data pad 132, thus reducing contact resistance. The transparent electrode material is formed from indium-tin-oxide (ITO), tin-oxide (TO) or indium-zinc-oxide (IZO).

[00075] As described above, according to the present invention, the data pad 132 is formed from a gate metal layer. Thus, the data pad 132 can be in surface contact with the data pad protection electrode 136 to reduce the contact resistance over that of the prior art (which used a side contact). As a result, it is possible to minimize a distortion of a pixel voltage signal caused by contact resistance.

[00076] Furthermore, according to the present invention, the data link portion adopts a parallel connection structure that is comprised of a gate metal layer and a transparent metal layer. This reduces the link resistance over the prior art that used single connection structure. As a result, the link resistance differences are reduced, thus reducing a distortion of pixel voltage signal caused by the link resistance difference.

[00077] Moreover, according to the present invention, the data pad is formed from a gate metal layer. Thus, erosion of the data pad can be prevented when a dry etching process removes the source/drain patterns and the ohmic contact layer. As a result, it is possible to reduce data pad defects, thereby improving manufacturing yield.

[00078] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.